CLAIMS

What is claimed is:

1. A fully depleted semiconductor-on-insulator (SOI) field effect transistor (FET), comprising:

a layer of semiconductor material disposed over an insulating layer, the insulating layer disposed over a semiconductor substrate;

a source and a drain formed from the layer of semiconductor material;

a body formed from the layer of semiconductor material and disposed between the source and the drain, wherein the layer of semiconductor material is etched such that a thickness of the body is less than a thickness of the source and the drain and such that a recess is formed in the layer of semiconductor material over the body; and

a gate formed at least in part in the recess and the gate defining a channel in the body, the gate including a gate electrode spaced apart from the body by a gate dielectric made from a high-K material.

2. The FET according to claim 1, wherein the body has a thickness of less than about 50 Å.

3. The FET according to claim 1, wherein a spacer is formed adjacent each sidewall of the gate electrode.

4. The FET according to claim 3, wherein each spacer is formed at least in part in the recess.

5. The FET according to claim 3, wherein each spacer is formed from an undoped polycrystalline silicon.

6. The FET according to claim 3, wherein the spacers are respectively separated from the source and the drain by an oxide layer.

7. The FET according to claim 3, wherein the spacers are separated from the gate electrode by the gate dielectric.

8. The FET according to claim 1, wherein the gate electrode is formed from a metal containing material.

9. The FET according to claim 8, wherein the gate electrode is composed of one or more materials selected from aluminum, ruthenium, ruthenium oxide and mixtures thereof.

10. The FET according to claim 1, wherein a source contact is disposed over the source, a drain contact is disposed over the drain and a TEOS oxide layer is formed over the source contact and the drain contact.

11. The FET according to claim 1, wherein the high-K material of the gate dielectric has a relative permittivity of greater than about 20.

12. The FET according to claim 1, wherein the high-K material of the gate dielectric is composed of one or more materials selected from hafnium oxide, zirconium oxide, cerium oxide, aluminum oxide, titanium oxide, yttrium oxide, barium strontium titanate and mixtures thereof.

13. A method of forming a fully depleted semiconductor-on-insulator (SOI) field effect transistor (FET), comprising:

providing a layer of semiconductor material, the layer of semiconductor material disposed over an insulating layer, and the insulating layer disposed over a semiconductor substrate;

forming a dummy gate on the layer of semiconductor material;

doping the layer of semiconductor material to form a source and a drain, and a body region between the source and the drain;

removing at least a portion of the dummy gate;

etching the layer of semiconductor material to form a recess therein, the recess formed in at least the body region of the layer of semiconductor material such that a thickness of the body is less than a thickness of the source and the drain; and

forming a gate at least in part in the recess and the gate defining a channel in the body, the gate including a gate electrode spaced apart from the body by a gate dielectric made from a high-K material.

14. The method according to claim 13, wherein the body has a thickness of less than about 50 Å.

15. The method according to claim 13, further comprising oxidizing the etched portion of the layer of semiconductor material prior to formation of the gate.

16. The method according to claim 15, further comprising forming a spacer in each lateral side of the recess and over the an oxide layer formed by the oxidation step, the spacers formed prior to formation of the gate.

17. The method according to claim 16, wherein each spacer is formed from an undoped polycrystalline silicon.

18. The method according to claim 16, further comprising removing a portion of the oxide layer between the spacers and wherein formation of the gate includes depositing a conformal layer of high-K material over the spacers and the body region of the layer of semiconductor material and depositing a layer of gate electrode material over the layer of high-K material.

19. The method according to claim 13, wherein removal of the at least a portion of the dummy gate results in the formation of spacers from the material of the dummy gate.

20. The method according to claim 13, wherein the gate electrode is formed from a metal containing material.

21. The method according to claim 13, further comprising siliciding the source and the drain to respectively form a source contact and a drain contact and forming a TEOS oxide layer over the source contact and the drain contact.

22. The method according to claim 13, wherein the high-K material of the gate dielectric is composed of one or more materials selected from hafnium oxide, zirconium oxide, cerium oxide, aluminum oxide, titanium oxide, yttrium oxide, barium strontium titanate and mixtures thereof.

23. The method according to claim 13, wherein etching of the layer of semiconductor material includes:

reactive ion etching to remove a first portion of the layer of semiconductor material;

wet etching to remove a second portion of the layer of semiconductor material; and

oxidizing the layer of semiconductor material to consume a third portion of the layer of semiconductor material.

24. The method according to claim 13, wherein etching of the layer of semiconductor material includes:

wet etching to remove a first portion of the layer of semiconductor material; and

oxidizing the layer of semiconductor material to consume a second portion of the layer of semiconductor material.